CLAIMS

What is claimed is:

1. A method of correcting impedance curvature in a MOS driver circuit, said method comprising:

using a first MOS transistor and second MOS transistor as part of said MOS driver circuit; and

operating said first MOS transistor and said second MOS transistor so as to compensate for changes in output impedance of said first MOS transistor through corresponding changes in output impedance of said second MOS transistor.

2. The method of claim 1, further comprising:

using a signal adder circuit as part of said MOS driver circuit,

wherein said operating comprises:

maintaining a controlled voltage at a first input terminal of said first MOS transistor, and

using said signal adder circuit to provide a differential voltage at a second input terminal of said second MOS transistor.

3. The method of claim 2, wherein said first and said second input terminals are respective gate terminals of said first and said second MOS transistors.

4. The method of claim 2, further comprising using an amplifier to provide an input signal to said signal adder circuit.

5. The method of claim 4, wherein using said amplifier includes using an output of said amplifier to supply said input signal to said signal adder circuit.

6. The method of claim 4, wherein said amplifier is a differential amplifier.

7. A method of correcting impedance curvature in a MOS driver circuit, said method comprising:

using a first MOS transistor and second MOS transistor as part of said MOS driver circuit; and

operating said first MOS transistor and said second MOS transistor so as to increase output impedance of said second MOS transistor when output impedance of said first MOS transistor decreases, and vice versa.

8. The method of claim 7, further comprising:

using a signal adder circuit as part of said MOS driver circuit,

wherein said operating comprises:

maintaining a controlled voltage at a first input terminal of said first MOS transistor, and

using said signal adder circuit to provide a differential voltage at a second input terminal of said second MOS transistor.

9. The method of claim 8, further comprising using a replica of said MOS driver circuit to supply an input signal to said signal adder circuit.

10. The method of claim 9, wherein said replica is a scaled replica of said MOS driver circuit.

11. The method of claim 9, wherein said operating further comprises:

using an amplifier to supply said controlled voltage to said first MOS transistor and also to a third input terminal of said replica of said MOS driver circuit.

12. The method of claim 11, wherein said amplifier includes a differential amplifier in an inverting configuration.

13. The method of claim 11, wherein using said amplifier further comprises using an output of said amplifier to supply said controlled voltage.

14. The method of claim 11, further comprising:

using said amplifier with at least two inputs; and

providing a reference voltage to at least one of said inputs of said amplifier.

15. The method of claim 9, wherein said signal adder circuit includes a differential amplifier.

16. The method of claim 15, wherein said input signal is supplied to an inverting input of said differential amplifier.

17. The method of claim 9, wherein using said replica includes using an output of said replica to supply said input signal to said signal adder circuit.

18. The method of claim 17, wherein using said replica further includes:

using a third MOS transistor as part of said replica; and

obtaining said output of said replica from a drain terminal of said third MOS transistor.

19. The method of claim 9, further comprising using a current reference to supply a current of predetermined value to said replica of said MOS driver circuit.

20. A method of correcting impedance curvature in a MOS driver circuit, said method comprising:

using a first MOS transistor and second MOS transistor as part of said MOS driver circuit;

using a signal adder circuit as part of said MOS driver circuit;

maintaining a controlled voltage at a first input terminal of said first MOS transistor;

using said signal adder circuit to provide a differential voltage at a second input terminal of said second MOS transistor; and

operating said first MOS transistor and said second MOS transistor so as to compensate for changes in output impedance of said first MOS transistor through corresponding changes in output impedance of said second MOS transistor.

21. The method of claim 20, wherein said operating further comprises:

using a first output terminal of said first MOS transistor to supply an input signal to said signal adder circuit, and

wherein using said signal adder circuit includes using an output of said signal adder circuit to provide said differential voltage to said second MOS transistor.

22. The method of claim 21, wherein said signal adder circuit is a differential amplifier, and wherein said input signal is supplied to a non-inverting input of said differential amplifier.

23. The method of claim 21, wherein said operating further comprises using said first output terminal along with a second output terminal of said second MOS transistor in series with a linearizing resistor.

24. The method of claim 23, wherein said linearizing resistor is integrally fabricated with said MOS driver circuit.

25. The method of claim 23, wherein nominal resistance of said linearizing resistor is in the range of 22 Ohms to 28 Ohms.

26. A method of correcting impedance curvature in a MOS driver circuit, said method comprising:

using a first MOS transistor and second MOS transistor as part of said MOS driver circuit;

using a signal adder circuit as part of said MOS driver circuit;

maintaining a controlled voltage at a first input terminal of said first MOS transistor;

using said signal adder circuit to provide a differential voltage at a second input terminal of said second MOS transistor; and

operating said first MOS transistor and said second MOS transistor so as to increase output impedance of said second MOS transistor when output impedance of said first MOS transistor decreases, and vice versa.

27. The method of claim 26, further comprising:

using a first amplifier to supply a first input signal to said signal adder circuit;

using a scaled replica of said MOS driver circuit to supply a second input signal to said first amplifier; and

using a second amplifier to supply said controlled voltage to a third input terminal of said scaled replica.

28. The method of claim 27, wherein said operating further comprises using said second amplifier to supply said controlled voltage to said first MOS transistor.

29. The method of claim 27, wherein said operating further comprises using said first amplifier to supply said controlled voltage to said first MOS transistor.

30. The method of claim 27, further comprising using a current reference to supply a current of predetermined value to said scaled replica of said MOS driver circuit.

31. The method of claim 30, wherein said predetermined value of said current from said current reference ranges from 0.68mA to 1mA.

32. A MOS driver circuit comprising:

a first MOS transistor configured to receive a controlled voltage at a first input terminal thereof; and

a second MOS transistor coupled to said first MOS transistor and configured to receive a differential voltage at a second input terminal thereof,

wherein said second MOS transistor is configured to have an increased output impedance when output impedance of said first MOS transistor decreases, and vice versa.

33. The MOS driver circuit of claim 32, wherein said first and said second input terminals are respective gate terminals of said first and said second MOS transistors.

34. The MOS driver circuit of claim 32, further comprising:

a signal adder circuit coupled to said first and said second MOS transistors, wherein a first output of said signal adder circuit is coupled to said second input terminal to provide said differential voltage to said second MOS transistor.

35. The MOS driver circuit of claim 34, wherein said signal adder circuit includes a differential amplifier.

36. The MOS driver circuit of claim 34, further comprising:

an amplifier having a second output coupled to said first input terminal to provide said controlled voltage to said first MOS transistor, wherein said amplifier further having a third output coupled to an input of said signal adder circuit to provide a bias voltage thereto.

37. A MOS driver circuit comprising:

a first MOS transistor configured to receive a controlled voltage at a first input terminal thereof; and

a second MOS transistor coupled to said first MOS transistor and configured to receive a differential voltage at a second input terminal thereof,

wherein said second MOS transistor is configured to compensate for changes in output impedance of said first MOS transistor through corresponding changes in output impedance of said second MOS transistor.

38. The MOS driver circuit of claim 37, further comprising:

a signal adder circuit coupled to said first and said second MOS transistors, wherein a first output of said signal adder circuit is coupled to said second input terminal to provide said differential voltage to said second MOS transistor.

39. The MOS driver circuit of claim 38, further comprising:

a scaled replica of said MOS driver circuit having a second output coupled to a first input of said signal adder circuit to provide a first input voltage thereto.

40. The MOS driver circuit of claim 39, wherein said first input is an inverting input of said signal adder circuit.

41. The MOS driver circuit of claim 39, wherein a first output terminal of said first MOS transistor is coupled to a second input of said signal adder circuit to provide a second input voltage thereto.

42. The MOS driver circuit of claim 41, wherein said second input is a non-inverting input of said signal adder circuit.

43. The MOS driver circuit of claim 41, wherein said first output terminal of said first MOS transistor and a second output terminal of said second MOS transistor are coupled in series with a linearizing resistor.

44. The MOS driver circuit of claim 43, wherein said first and said second output terminals are respective drain terminals of said first and said second MOS transistors.

45. The MOS driver circuit of claim 43, wherein said linearizing resistor is integrally fabricated with said first and said second MOS transistors, and wherein nominal resistance of said linearizing resistor is in the range of 22 Ohms to 28 Ohms.

46. A MOS driver circuit comprising:

a first MOS transistor configured to receive a controlled voltage at a first input terminal thereof; and

a second MOS transistor coupled to said first MOS transistor and configured to receive a differential voltage at a second input terminal thereof, wherein said second MOS transistor is configured to have an increased output impedance when output impedance of said first MOS transistor decreases, and vice versa;

a signal adder circuit coupled to said first and said second MOS transistors, wherein a first output of said signal adder circuit is coupled to said second input terminal to provide said differential voltage to said second MOS transistor, and wherein a

first output terminal of said first MOS transistor is coupled to a first input of said signal adder circuit to provide a first input voltage thereto;

a scaled replica of said MOS driver circuit having a second output coupled to a second input of said signal adder circuit to provide a second input voltage thereto; and

a linearizing resistor coupled in series with said first output terminal of said first MOS transistor and a second output terminal of said second MOS transistor.

47. The MOS driver circuit of claim 46, wherein said scaled replica includes a third MOS transistor, wherein a third output terminal of said third MOS transistor is configured to function as said second output.

48. The MOS driver circuit of claim 47, wherein said first, said second, and said third MOS transistors are CMOS transistors.

49. The MOS driver circuit of claim 47, wherein said third output terminal is a drain terminal of said third MOS transistor.

50. The MOS driver circuit of claim 47, wherein source terminals of said first, said second, and said third MOS transistors are held at a common reference potential.

51. The MOS driver circuit of claim 47, further comprising a current reference coupled to said third output terminal of said third MOS transistor.

52. The MOS driver circuit of claim 47, further comprising:

a first amplifier having a third output coupled to a third input terminal of said third MOS transistor to supply said controlled voltage to said third input terminal; and

a second amplifier coupled to said third MOS transistor and said first MOS transistor, wherein said second amplifier is configured to provide said controlled voltage to said first input terminal of said first MOS transistor.

53. A MOS driver circuit comprising:

a first MOS transistor configured to receive a controlled voltage at a first input terminal thereof;

a second MOS transistor coupled to said first MOS transistor and configured to receive a differential voltage at a second input terminal thereof, wherein said second MOS transistor is configured to compensate for changes in output impedance of said first MOS transistor through corresponding changes in output impedance of said second MOS transistor;

a signal adder circuit coupled to said first and said second MOS transistors, wherein a first output of said signal adder circuit is coupled to said second input terminal to provide said differential voltage to said second MOS transistor, and wherein a first output terminal of said first MOS transistor is coupled to a first input of said signal adder circuit to provide a first input voltage thereto;

a scaled replica of said MOS driver circuit having a second output coupled to a second input of said signal adder circuit to provide a second input voltage thereto; and

a linearizing resistor coupled in series with said first output terminal of said first MOS transistor and a second output terminal of said second MOS transistor.

54. The MOS driver circuit of claim 53, wherein said scaled replica includes a third MOS transistor, wherein a third output terminal of said third MOS transistor is configured to function as said second output.

55. The MOS driver circuit of claim 54, further comprising:

a first amplifier having a third output coupled to a third input terminal of said third MOS transistor and said first input terminal of said first MOS transistor to supply said controlled voltage to said first and said third input terminals.

56. The MOS driver circuit of claim 55, wherein said first amplifier is an inverting differential amplifier.

57. The MOS driver circuit of claim 55, wherein said first amplifier has at least two inputs, and wherein at least one of said at least two inputs is held at a reference potential.

58. The MOS driver circuit of claim 55, wherein an input of said first amplifier and said third output terminal of said third MOS transistor are coupled to a DC supply voltage.

59. The MOS driver circuit of claim 55, further comprising:
a second amplifier connected between said second output of said scaled replica and said second input of said signal adder circuit, wherein said second amplifier is configured to provide said second input voltage to said signal adder circuit.

60. A method of operating a MOS driver circuit, said method comprising:
using a first MOS transistor with a first terminal, a second terminal, and a third terminal;
using a second MOS transistor with a fourth terminal, a fifth terminal, and a sixth terminal;
providing a DC supply voltage to said first and said fourth terminals;
further providing a reference potential to said second and said fifth terminals; and
further using an internal linearizing resistor and an external precision resistor in series with said third and said sixth terminals.

61. The method of claim 60, wherein said further using includes:
deactivating a portion of said internal linearizing resistor during operation of said MOS driver circuit.

62. The method of claim 60, wherein said further using includes using only a portion of said internal linearizing resistor in series with said third and said sixth terminals.

63. The method of claim 62, wherein said portion of said internal linearizing resistor has a nominal value of 8 Ohms, and wherein said external precision resistor has a nominal value of 22 Ohms.

64. A system comprising:
a processor;

a memory controller;

a memory device;

a first bus interconnecting the processor and the memory controller; and

a second bus interconnecting the memory controller and the memory device,

wherein at least one of said processor, said memory controller, and said memory device includes a MOS driver circuit having:

a first MOS transistor configured to receive a controlled voltage at a first input terminal thereof, and

a second MOS transistor coupled to said first MOS transistor and configured to receive a differential voltage at a second input terminal thereof, wherein said second MOS transistor is configured to compensate for changes in output impedance of said first MOS transistor through corresponding changes in output impedance of said second MOS transistor.

65. A system comprising:

a data processing unit including:

a processor,

a memory controller,

a memory device,

a first bus interconnecting the processor and the memory controller, and

a second bus interconnecting the memory controller and the memory device;

an input device connected to said data processing unit;

an output device connected to said data processing unit; and

a data storage device connected to said data processing unit,

wherein at least one of said processor, said memory controller, said memory device, said input device, said output device, and said data storage device includes a MOS driver circuit having:

a first MOS transistor configured to receive a controlled voltage at a first input terminal thereof, and

a second MOS transistor coupled to said first MOS transistor and configured to receive a differential voltage at a second input terminal thereof, wherein

said second MOS transistor is configured to have an increased output impedance when output impedance of said first MOS transistor decreases, and vice versa.